Claims

What is claimed is:

1. An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a dielectric substrate mounted on the first side of the conductive trace layer;

a capacitor including a first conductive layer, a second conductive layer and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

2. The electronic package of claim 1 wherein the first electrode is maintained at a first reference voltage and wherein the second electrode is maintained at a second reference voltage different from the first reference voltage.

3. The electronic package of claim 1 further comprising an electrically conductive stiffening member mounted adjacent to the second conductive layer of the capacitor.

4. The electronic package of claim 3 further comprising a device receiving region extending through the dielectric substrate, the conductive trace layer and the

capacitor, and further comprising an electronic device mounted in the device receiving region on the stiffening member.

5. The electronic package of claim 4 wherein the electronic device includes a plurality of bonding pads, and further comprises a first wire electrically connected between a first one of the bonding pads and the first conductive layer of the capacitor, and a second wire electrically connected between a second one of the bonding pads and the second conductive layer of the capacitor.

6. The electronic package of claim 4 wherein the electronic device includes a plurality of bonding pads, and further comprises a first wire electrically connected between a first one of the bonding pads and the first conductive layer of the capacitor, and a second wire electrically connected between a second one of the bonding pads and the stiffening member.

7. The electronic package of claim 6 further comprising an electrically conductive adhesive disposed between the second conductive layer of the capacitor and the stiffening member.

8. The electronic package of claim 1 wherein the capacitor has a capacitance of from about 2 nF/sq. cm. to about 30 nF/sq. cm.

9. The electronic package of claim 1 wherein the capacitor has a capacitance of from about 5 nF/sq. cm. to about 15 nF/sq. cm.

10. The electronic package of claim 1 wherein the capacitor has a capacitance of at least 30nF/sq. cm.

11. The electronic package of claim 1 wherein the dielectric material of the capacitor has a thickness of from about 5 um to about 30 um.

12. The electronic package of claim 1 wherein the dielectric material of the capacitor includes a metal oxide.

13. The electronic package of claim 1 wherein the dielectric material is made of a non-conductive polymer blended with high dielectric constant particles, the high dielectric constant particles having been formed from a material selected from the group consisting of barium titinate, barium strontium titinate, titanium oxide, lead zirconium titinate and tantalum oxide.

14. The electronic package of claim 1 wherein the dielectric substrate includes a plurality of apertures, each one of the apertures being positioned adjacent to one of the interconnect region of the capacitor.

15. The electronic package of claim 1 wherein the dielectric substrate includes a polymeric film.

16. The electronic package of claim 15 wherein said polymeric film is polyimide film.

17. The electronic package of claim 1 wherein the interconnect member is a solder plug.

18. The electronic package of claim 1 wherein each interconnect pad is a solderball pad.

19. The electronic package of claim 1 wherein the dielectric substrate has an aperture extending therethrough adjacent to each solderball pad.

20. An electronic package, comprising:

a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads;

a flexible dielectric substrate mounted on the first side of the conductive trace layer;

a flexible capacitor including a first conductive layer, a second conductive layer and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer;

a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor; and

an interconnect member connected between each one of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer of the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions;

an aperture extending through the dielectric substrate adjacent to each one of the interconnect pads;

a stiffening member mounted adjacent to the second conductive layer of the capacitor; and

a device receiving region formed through the dielectric substrate, the conductive trace layer and the capacitor.

21. A method of reducing impedance in an electronic package, comprising the steps of:

forming an interconnect circuit including a conductive trace layer patterned to define a plurality of interconnect pads and a dielectric substrate mounted on a first side of the conductive trace layer;

forming a capacitor including a first conductive layer, a second conductive layer and a layer of dielectric material disposed between the first and the second conductive layers;

forming a plurality of openings through the first conductive layer and the layer of dielectric material of the capacitor to define a plurality of interconnect regions;

mounting the capacitor on the interconnect circuit with the first conductive layer of the capacitor adjacent to a second side of the conductive trace layer; and

electrically interconnecting the first conductive layer of the capacitor with a first set of the interconnect pads and the second conductive layer of the capacitor with a second set of the interconnect pads.

22. The method of claim 21 wherein the step of electrically interconnecting the second conductive layer with the second set of interconnect pads includes the steps of connecting an interconnect member between the second set of interconnect pads and the second conductive layer, and extending the interconnect members through one of the interconnect regions.

23. The method of claim 21 further comprising the step of mounting an electrically conductive stiffening member on the second conductive layer of the capacitor including the step of forming a layer of electrically conductive adhesive between the stiffening member and the second conductive layer of the capacitor..

24. The method of claim 23 further comprising the step of forming a device receiving region through the dielectric substrate, the conductive trace layer and the capacitor, and mounting an electronic device in the device receiving region on the stiffening member.

25. The method of claim 24 further comprising the steps of: (a) electrically connecting a first wire between a first bonding pad of the electronic device and the first conductive layer of the capacitor, and electrically connecting a second wire between a second bonding pad of the electronic device and the second conductive layer of the capacitor, and (b) electrically connecting a first wire between a first bonding pad of the electronic device and the first conductive layer of the capacitor, and electrically connecting a second wire between a second bonding pad of the electronic device and the stiffening member.

26. The method of claim 21 wherein the step of forming the interconnect circuit includes the step of forming a plurality of apertures in the dielectric substrate adjacent to each one of the interconnect pads.